III. REMARKS

Claims 1-10 are pending in this application. Applicant does not acquiesce in the correctness of the rejections and reserves the right to present specific arguments regarding any rejected claims not specifically addressed. Further, Applicant reserves the right to pursue the full scope of the subject matter of the original claims in a subsequent patent application that claims priority to the instant application. Reconsideration in view of the following remarks is respectfully requested.

In the Office Action, claims 1-10 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Pawloski (U.S. Patent No. 5,426,769), hereafter "Pawloski" in view of Dallas Semiconductor "DS87C550 Product Preview," hereafter "Dallas."

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Applicant respectfully submits that the Pawloski and Dallas references, taken alone or in combination, fail to meet each of the three basic criteria required to establish a *prima facie* case of obviousness. As such, the rejection under 35 U.S.C. 103(a) is defective.

Specifically, Applicant asserts that the combined references cited by the Office fail to teach or suggest each and every feature of the claimed invention. For example, with respect to independent claims 1 and 10, Applicant submits that the cited references fail to teach or suggest a control register that is instruction-settable to respective control states that control whether or not

the processing device updates the at least two addresses as a side-effect of executing the memory access instruction. The Office expressly states that Dallas Semiconductor does not disclose such a control register. Instead, the Office erroneously attempts to equate the control SFR in Pawloski with the control register as included in the claimed invention. However, the control SFR (special function register) in Pawloski is used in conjunction with an external expansion device that Pawloski allows the system to access. Col. 13, line 62 through col. 14, line 6. One type of external system that may be accessed by the Pawloski system is called an expanded 8051 internal data memory. Col. 14, lines 22-25. This data memory contains 1024 bytes that are preferably divided into four pages of 256 bytes each, with each page having a 128-byte address SFR and a 128-byte data SFR. Col. 14, lines 39-47. Each of the pages may also have a control SFR, which has one or more bits that are used to enable and disable the auto increment or auto decrement function of the address SFR. Col. 14, lines 46-61. However, the Pawloski control SFR is located on an external expansion device, not in the processor itself. Furthermore, the control SFR in Pawloski enables and disables an auto increment or auto decrement function of an address SFR field, and does not control whether or not the processor changes which one of the at least two parallel addresses is accessed. Nowhere does Pawloski teach that its SFR control is a local control that controls whether or not the processor changes which one of the at least two parallel addresses is accessed. In contrast, the present invention includes "...a control register that is instruction-settable to respective control states that control whether or not the processing device updates the at least two addresses as a side-effect of executing the memory access instruction." Claim 1. As such, the control as included in the claimed invention is not a part of an external expansion device as is the SFR control in Pawloski, but is rather, *inter alia*, in a local

control register. Furthermore, unlike the control SFR in Pawloski, which enables and disables an address auto increment and auto decrement function, the control states as included in the claimed invention control whether or not the processing device updates the at least two addresses as a side-effect of executing the memory access instruction. Thus, the functions performed by the control register as included in the present invention are not equivalent to the control SFR in Pawloski. Accordingly, Applicant respectfully requests that the Office withdraw its rejection.

With further respect to independent claims 1 and 10, Applicant asserts that there is no motivation to combine the Pawloski and Dallas references. Even if, *arguendo*, Pawloski teaches a control register as argued by the Office, the Dallas reference describes an integrated chip microcontroller. Description section of Dallas. The SFR control in Pawloski, in contrast, is located in an expansion memory that is external to the Pawloski processor. Col. 13, line 62 through col. 14, line 6. Thus, there would be no motivation to combine the external SFR control in Pawloski with Dallas's integrated microcontroller. Accordingly, Applicant respectfully requests withdrawal of this rejection.

With regard to the Office's other arguments regarding dependent claims, Applicant herein incorporates the arguments presented above with respect to independent claims listed above. In addition, Applicant submits that all dependant claims are allowable based on their own distinct features. However, for brevity, Applicant will forego addressing each of these rejections individually, but reserves the right to do so should it become necessary. Accordingly, Applicant respectfully requests that the Office withdraw its rejection.

IV. CONCLUSION

In light of the above, Applicant respectfully submits that all claims are in condition for allowance. Should the Examiner require anything further to place the application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the number listed below.

Respectfully submitted,

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